Access to Advanced Packaging and Test
4:00 pm – 5:45 pm

Introduction

Brett Hamilton, Naval Surface Warfare Center (NSWC) Crane, Advanced Packaging and Test, Technical Execution Lead

Panel Members:

- Meredith Anderson Dyck, PhD, Acting Technical Director, NSA Laboratory for Physical Sciences
- Frank Ferrante, Director Military, Aerospace and Government, Intel PSG
- Radoslav (Rocco) Bogoslovov, PhD, Principle Scientist, SETA, DARPA MTO
- Sarah Leeper, Director, Secure & Assured Systems, Draper
- Steven Dooley, Senior Engineer, AFRL Sensors Directorate

Q&A - Discussion

Brett Hamilton

Mr. Brett Hamilton was promoted to the rank of Senior Scientific Technical Manager (SSTM) and assumed the duties as the DoN's Distinguished Scientist for Trusted Microelectronics in Oct 2017. In this role Mr. Hamilton oversees full spectrum life cycle of scientific and engineering functions in research, design, development, testing, and evaluation of microelectronics, areas where he holds multiple patents. He routinely advises senior leadership regarding issues involving microelectronics trust and integrity, including testimony before the House Armed Services Committee on Oversight and Investigations and was recently designated as the principal lead for heterogeneous packaging within the Office of the Under Secretary of Defense for Research and Engineering (OUSD(R&E)).

Heterogeneous Packaging and Test Panel Intro

Brett Hamilton
Heterogeneous Packaging and Test Panel

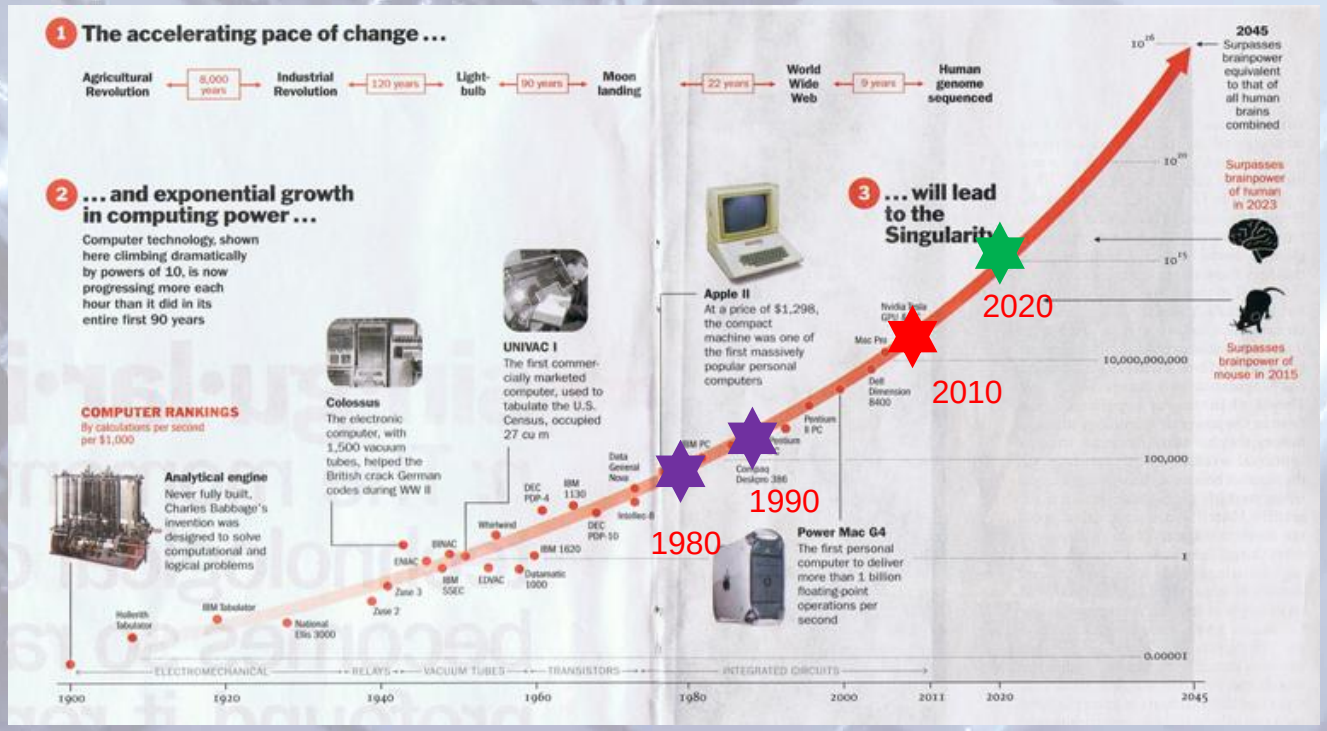
DARPA ERI, T&AM Workshop

Thursday, August 20, 2020

https://www.CTO.mil @DoDCTO

WHY Access to SOTA Microelectronics is Important - Being a Decade Behind Matters More Now

Exponential Growth + Emerging Needs + Near Peer Adversary = Loss of Advantage



US navy makes history by landing unmanned drone on aircraft carrier

https://www.theguardian.com/world/video/2013/jul/11/drone-aircraft-carrier-video

China unveils high-tech stealth drone concept

https://www.asiatimes.com/2019/07/article/chinas-flying-wing-stealth-drone-concept-unveiled/

World Leaders

Industry Giants TSMC and Intel Vow to Focus on 3D IC Packaging [(1)]

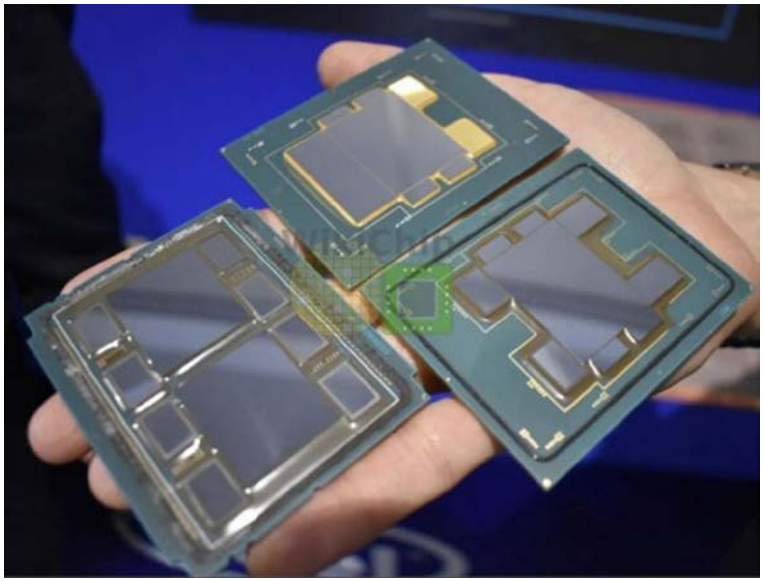
Demand for high-performance computing (HPC) chips is exploding. These super-speedy chips are critical for data centers and cloud computing infrastructures to support new performance-hungry technologies such as artificial intelligence (AI) and 5G……. Heterogeneous integration offers a potential answer as an advanced packaging technology designed to meet these skyrocketing performance demands on HPC chips and open the door to a whole new world of 3D integrated circuits (ICs).

So important are 3D ICs that Intel and TSMC representatives speaking at the recent Heterogeneous Integration Summit hosted by SEMI Taiwan in Taipei declared that the packaging technology will all but dictate the future of the industry.

Source: Intel – Accelerating Innovation Through Chiplets OCP/ODSA Workshop, 6/10/2019

[(1)] https://blog.semi.org/technology-trends/industry-giants-tsmc-and-intel-vow-to-focus-on-3d-ic-packaging

This Technology is Commercially Available



Intel revealed three new packaging technologies at SEMICON West: Co-EMIB, Omni-Directional Interconnect (ODI) and Multi-Die I/O (MDIO). These new technologies enable massive designs by stitching together multiple dies into one processor. Building upon Intel's 2.5D EMIB and 3D Foveros tech, the technologies aim to bring near-monolithic power and performance to heterogeneous packages.

https://www.tomshardware.com/news/intel-packaging-co-emib-odi-foveros-mdio,39840.html

NEC's Latest Vector Processor - The chip utilizes **TSMC**'s second-generation chip on wafer on substrate (CoWoS) technology with NEC's implementation developed in collaboration with TSMC and Broadcom.

https://fuse.wikichip.org/news/1833/a-look-at-necs-latest-vector-processor-the-sx-aurora/2/

DoD Research and Engineering Enterprise

Creating the Technologies of the Future Fight

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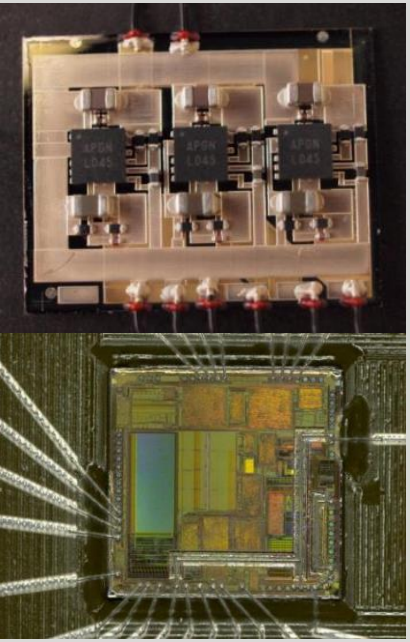
Q&A - Discussion

Dr. Meredith Anderson Dyck

Dr. Meredith Anderson Dyck is the Acting Technical Director of the Laboratory for Physical Sciences within NSA's Research Directorate. Dr. Dyck earned her Ph.D. in Physics from Carnegie Mellon University in 2004. Upon graduation, she joined Sandia National Laboratories as a principle investigator and program lead for USG customers in the areas of hardware inspection and characterization for trusted microelectronics. In 2019, Dr. Dyck joined NSA/LPS, which houses significant capabilities and expertise in additive manufacturing, sensing, quantum information science, and advanced high-performance computing systems. In this role, she guides the research and development of science-based solutions and technology transfer of those outputs to solve complex challenges that face the Defense and Intelligence Communities.

Printed Hybrid Electronics (PHE) SHIP Program



Meredith Dyck, PhD
Acting Technical Director

NSA, Laboratory for Physical Sciences

ERI: Heterogeneous Packaging & Test Panel

August 20, 2020

Printed Hybrid Electronics Motivation

PHE combines traditional circuit components and direct-write printing methods to fabricate novel electronic components and systems with unique form factors.

Advantages:

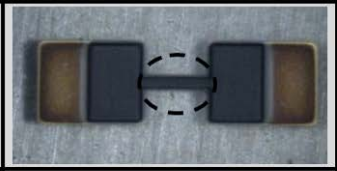
- Non-flat and flexible form factors
- Rapid production
- Ease of integration

Applications:

- Multi Chip Modules
- Rapid Prototyping PCB's
- Sensors
- RF circuit components

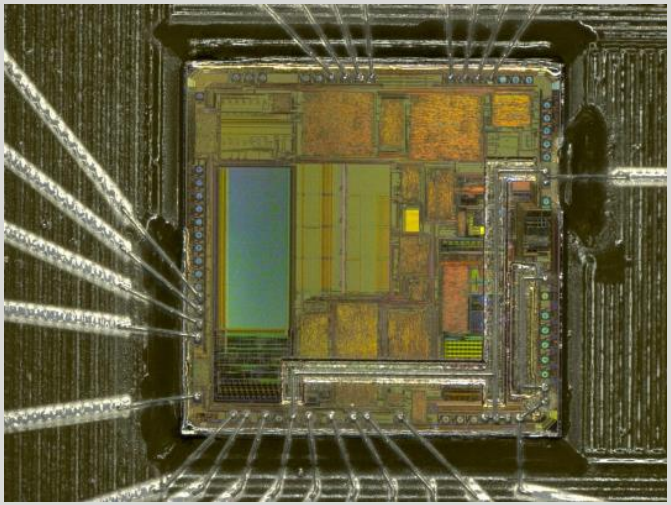
Print what you can. Place what you can't.

Examples

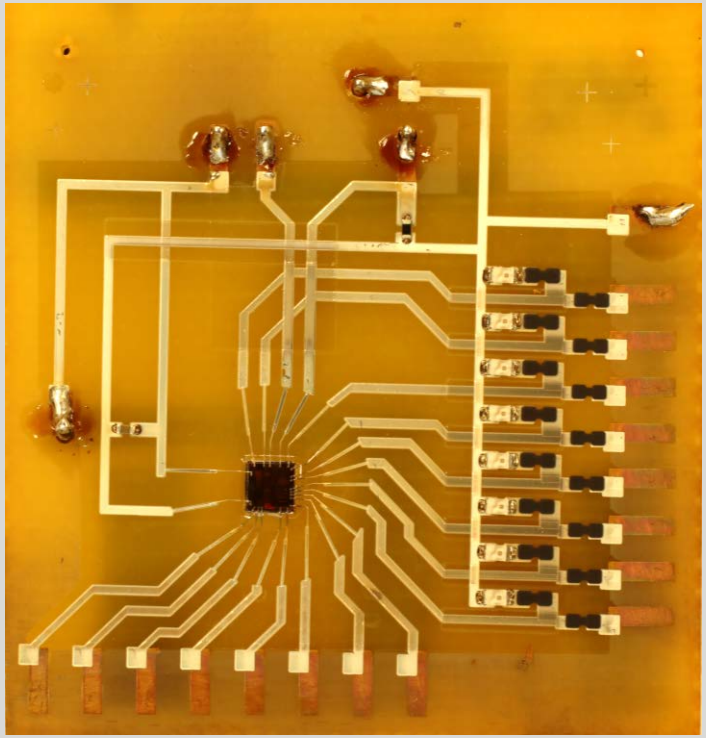
Components	Standard	PHE
Integrated Circuit Packaged vs. Bare Die		
Resistor Surface Mounted vs. Printed		
Capacitor Surface Mounted vs. Si based bare die		

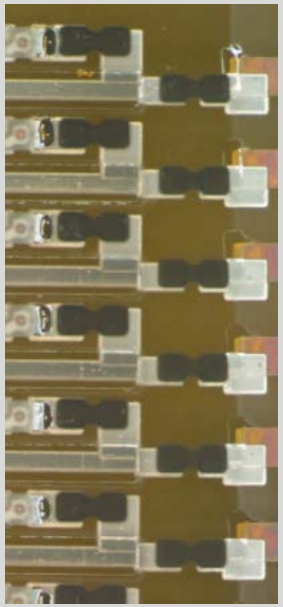
2D PHE Microcontroller Circuit

PHE Micro-Controller Circuit: Aerosol Jet-Printed with Integrated (Bare) Controller Chip



Si chip out of the package with Printed Interconnects

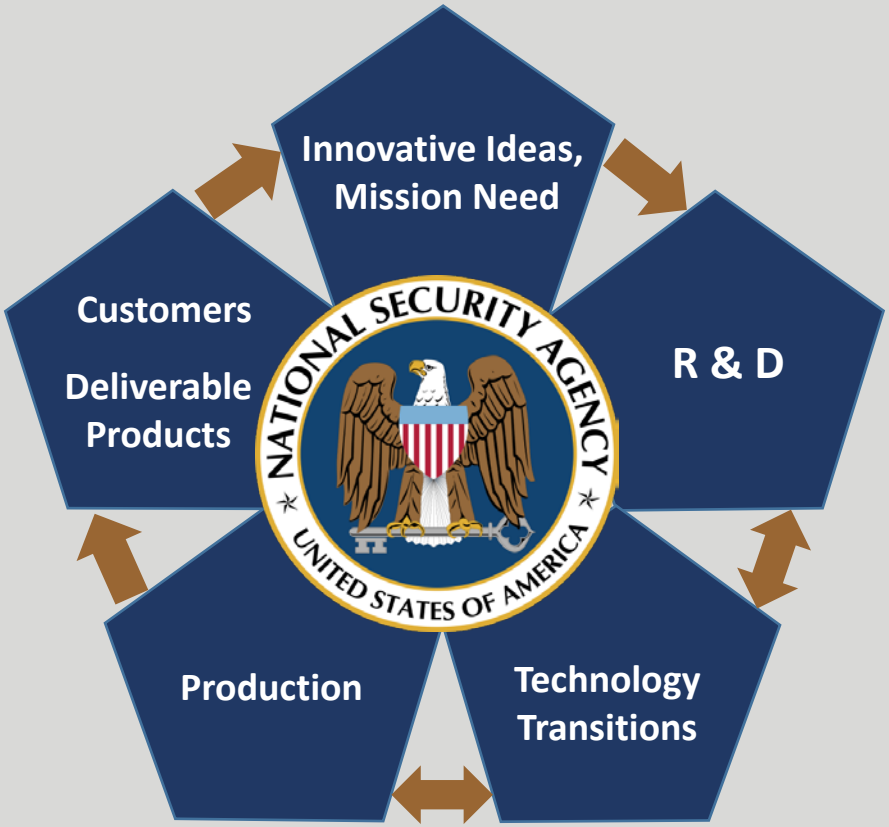




Printed Resistors

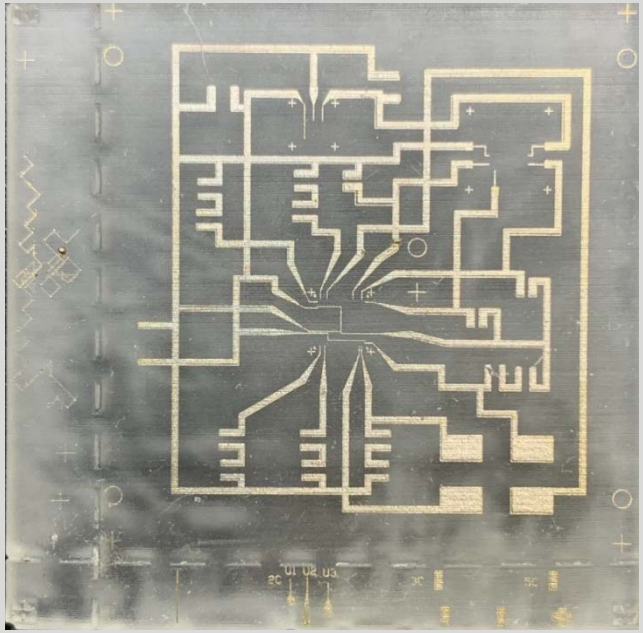
SHIP-PHE Program Goals

- **Leverage** previous work and existing infrastructure investments.
- **Mature** printed electronics technology into a small volume production capability for the USG.
- **Technology transfer** across DoD and industry to contribute to domestic, Advanced Manufacturing Ecosystem.



SHIP-PHE: Phase 1

SHIP PHE 'Arduino' Circuit Conducting Layers Test Print



Total Print Time for all conducting layers ~ 2hrs

Layer Stack

Circuitization 2

Dielectric 1

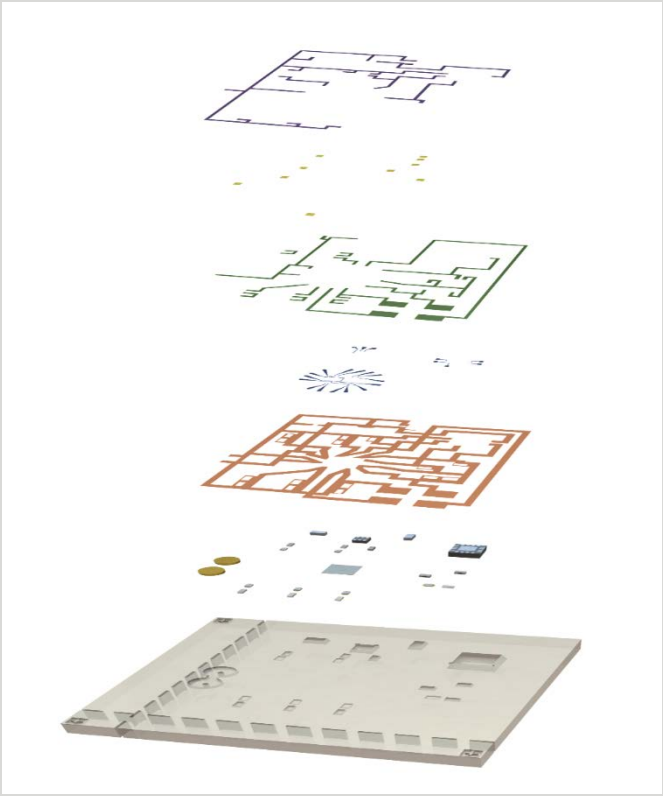
Circuitization 1

Interconnects

Base Dielectric

Components

3D Printed (30.5 x 31.5) mm Substrate containing cavities for component mounting.



Phase 2: Printed Multi Chip Modules

Std. Wire Bond Version

Printed Version

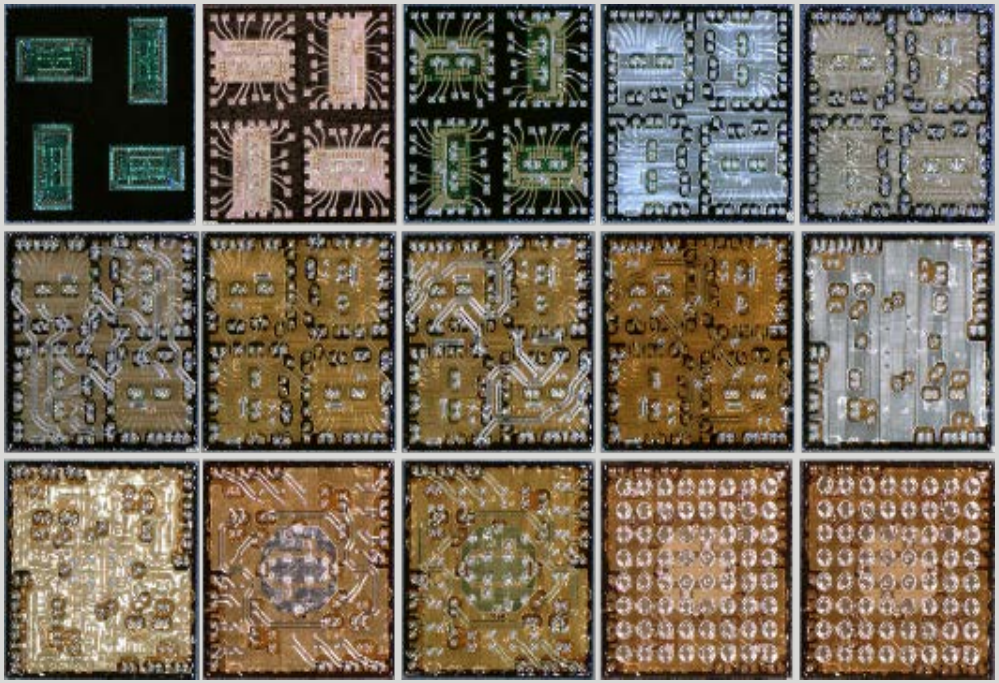
Multi Chip Module (MCM)

- 4 chips in a 4.3 Sq. mm area
- 14 printed sub-layers in the printed Redistribution Layer

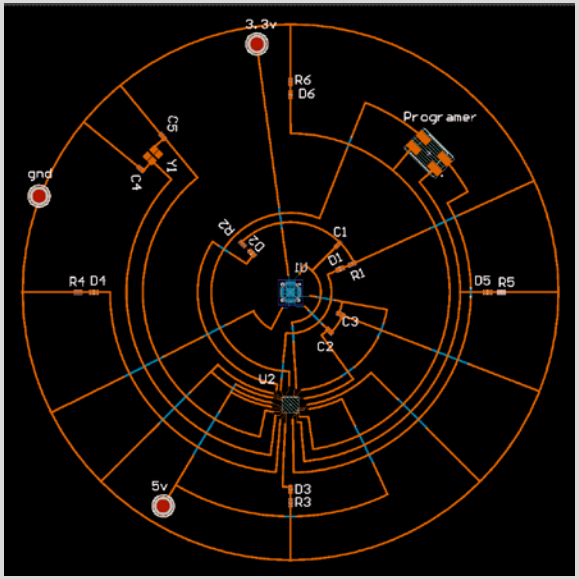
Printing & Processing Requirements:

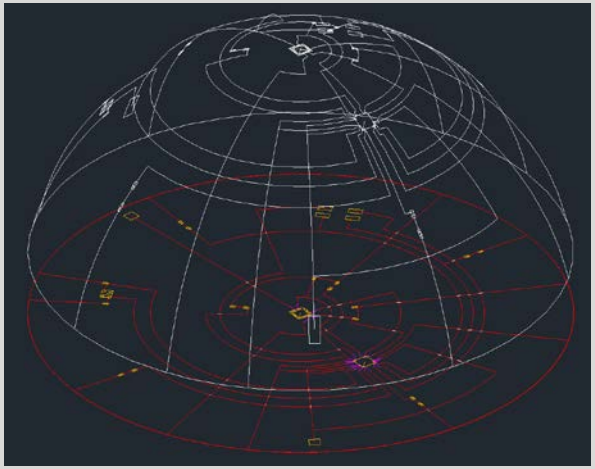
- < 1 Hour Printing + Processing time per Layer
- Compatible with Reflow Oven Processing Temperatures or Lower
- Resistivity < 4x Bulk Ag

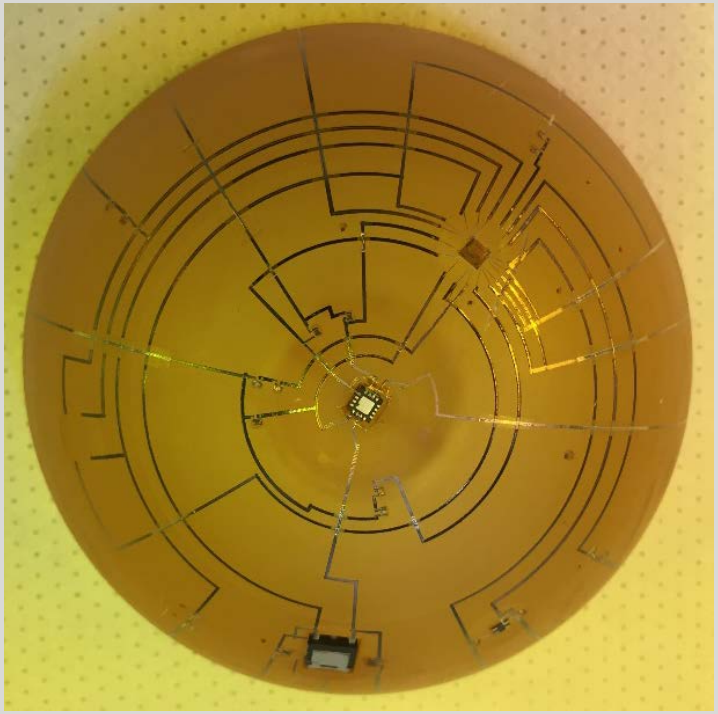
Printed Sub-Layers of the Redistribution Layer



Phase 3: Conformal Printed Electronics







PHE ‘Arduino’ on a 4”, 3D printed, Hemispherical Surface


National Security Agency
Laboratory for Physical Sciences
www.nsa.gov
www.lps.gov
meredith@lps.gov

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- Steven Dooley, Senior Engineer, AFRL Sensors Directorate

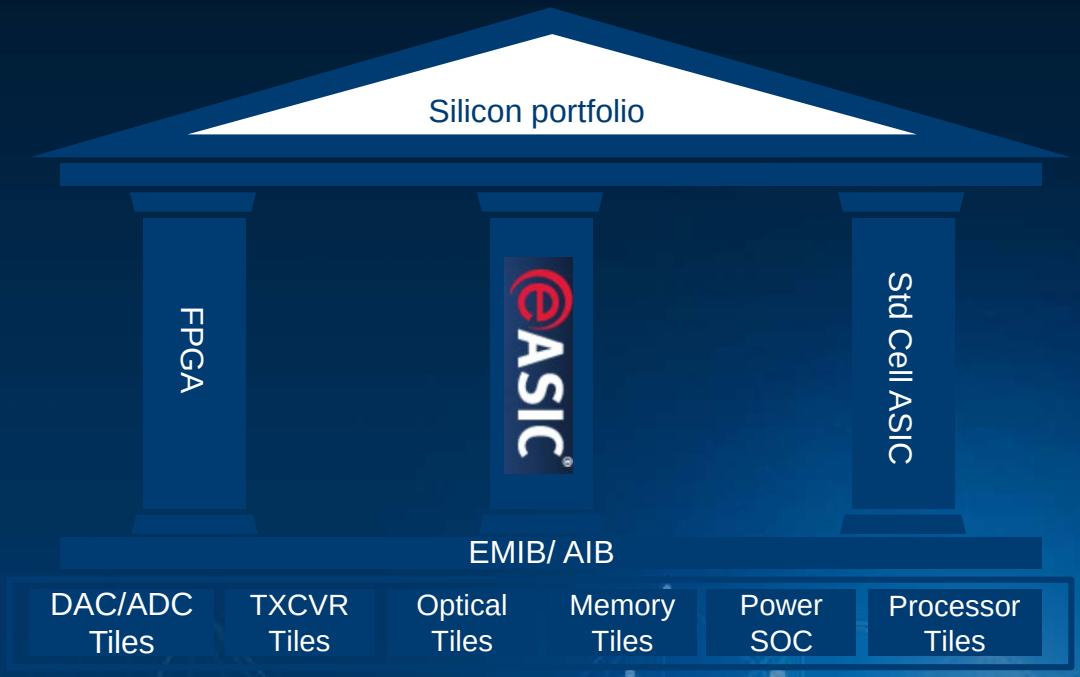
Q&A Discussion

Frank Ferrante

Frank Ferrante is responsible for the Military Aerospace and Government division of Intel PSG. He has been with Altera/Intel since 2008 and worked on communication systems, AI for Automotive and for the last couple of years on Military Solutions. His team of architects are working on Heterogeneous Solutions incorporating Intel and other company's die into Multichip Packages.


intel
Intel PSG Mag
Programmable solutions Group

Scalable Platform Strategy



Enable silicon programmability and hardened customization

- ✓ Optimized by market
- ✓ Further optimized by customer
- ✓ Tailored capability to desired combination of TTM, cost, power, integration

Reduce customer's R&D spend

- ✓ Consistent IP across pillars
- ✓ Software and package compatibility
- ✓ Maximizes reuse

Mix and match pillars and tiles

- ✓ Leverage chiplet strategy to integrate independent of node
- ✓ Blend pillar components for optimal power, performance, cost


intel
Thank You

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Q&A - Discussion

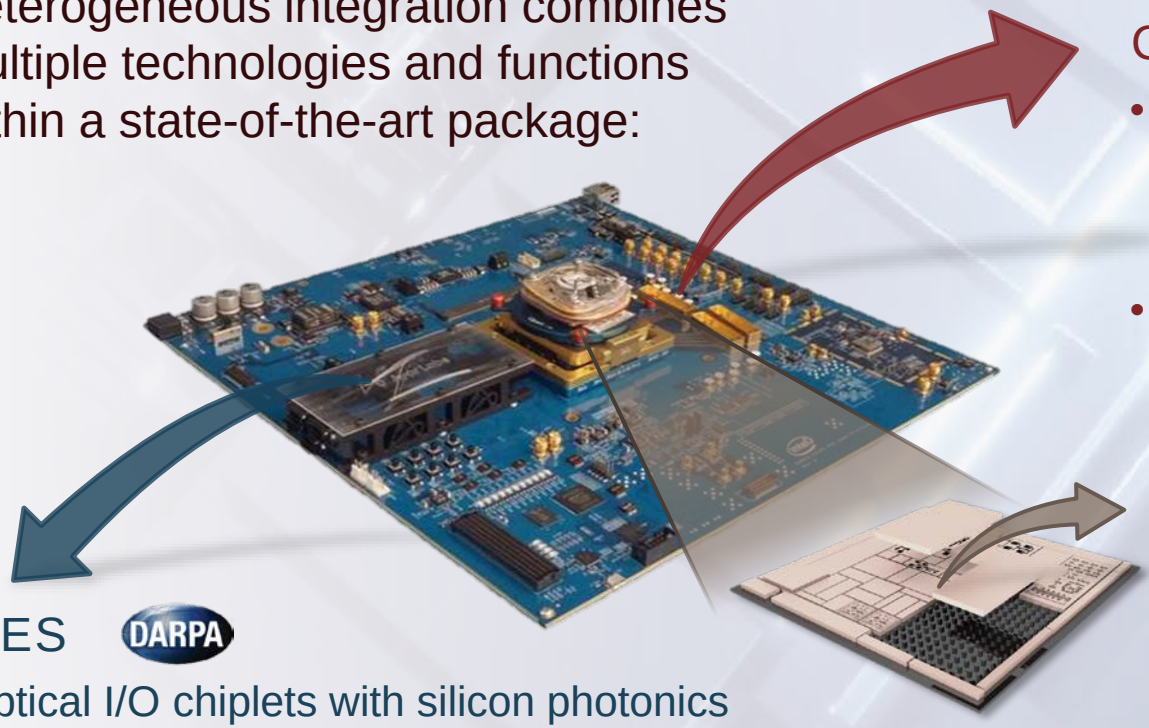
Dr. Radoslav Bogoslovov

Dr. Bogoslovov received his Ph. D. in physics from University of Nevada, Las Vegas, followed by postdoctoral work at the Naval Research Lab in Washington, DC. Dr. Bogoslovov has worked as a scientific and engineering consultant at DARPA MTO for the last 8 years. He worked on programs in optics and photonics, sensing and RF communications. Presently, Dr. Bogoslovov is supporting a portfolio of programs in microelectronics and photonics, including DARPA CHIPS and PIPES. Dr. Bogoslovov is a Senior Member of the IEEE and a Member of the OSA.

CO-PACKAGING HETEROGENEOUS MICROELECTRONICS AND OPTICAL I/O

3DHI – MAIN STAGE SESSION SUMMARY

Heterogeneous integration combines multiple technologies and functions within a state-of-the-art package:



CHIPS

- FPGA integration with:
  - RF data converters
  - Optical I/O
  - ML, DSP accelerators
- Fine pitch Si-IF for massive scalability

SHIP

- On-shore heterogeneous integration and advanced packaging

PIPES

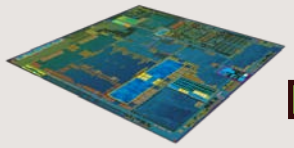
- Optical I/O chiplets with silicon photonics
- Optical fiber enabled MCMs

Images from DARPA CHIPS, Intel/Ayar Labs

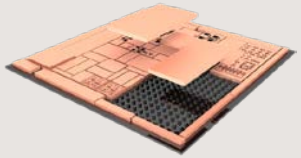
CHIPS

COMMON HETEROGENEOUS INTEGRATION AND IP REUSE STRATEGIES

DESIGN



Today:
monolithic

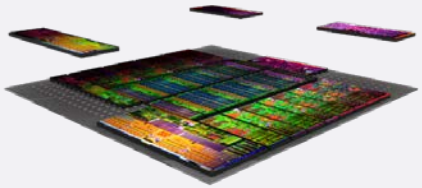


Tomorrow:
pseudolithic +
heterogeneous

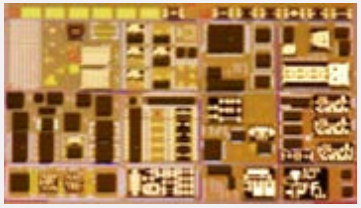
Image source: Intel

TECHNOLOGY

- ✓ **A universal efficient interface standard**
- ✓ **SOTA manufacturing assembly**
- ✓ **A large and critical set of IP chiplets**



Extend Moore's law
Scale out and scale down while managing yield

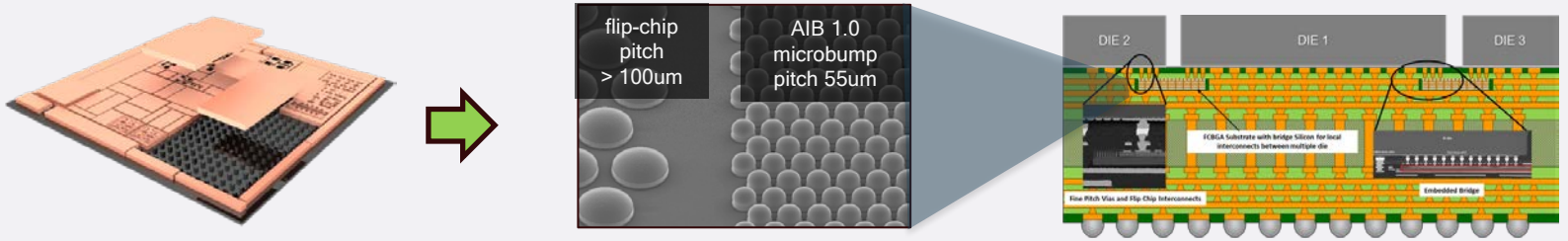


Enable heterogeneous integration
Materials/processes, companies, geography, security

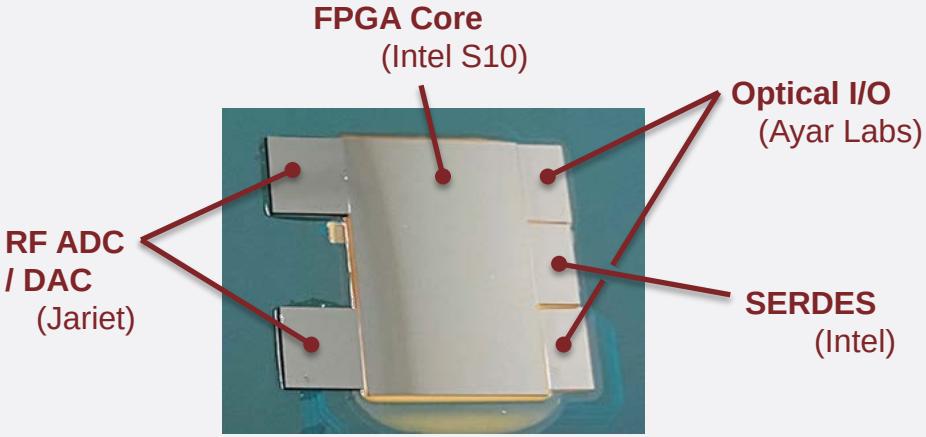
Empower system integrators
Democratize access to leading edge silicon for system integrators

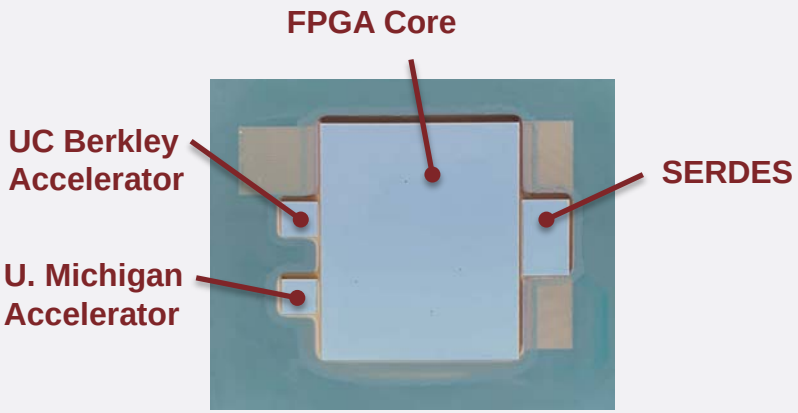
CHIPS HIGHLIGHTS 1

ORGANIC SUBSTRATE WITH AN EMBEDDED INTERPOSER



Intel Embedded Multi-Die Interconnect Bridge (EMIB)

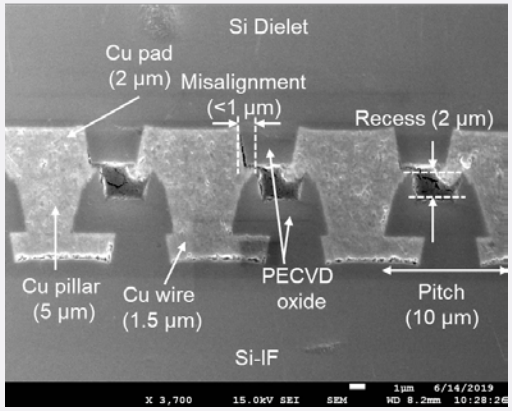


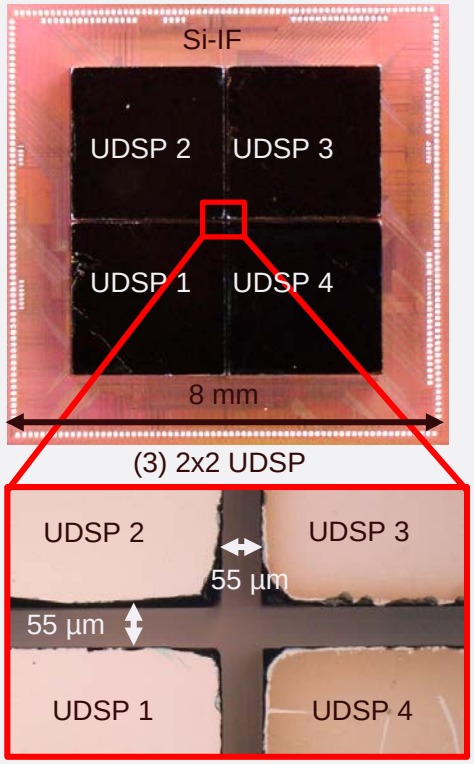


All images courtesy of Intel

CHIPS HIGHLIGHTS 2

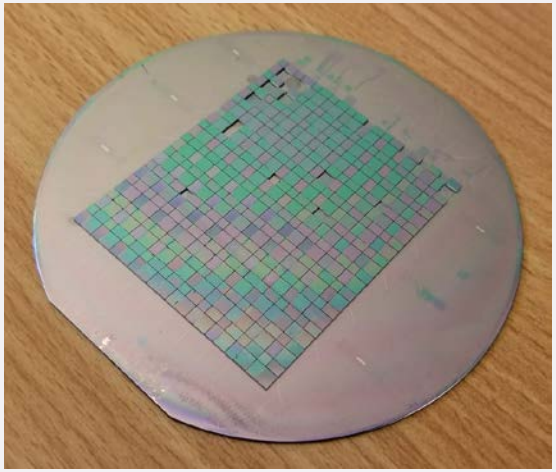
SI-IF: SILICON INTERCONNECT FABRIC (UCLA)





- 10 µm bump pitch
- <1 µm alignment
- 55 µm inter-die spacing
- TSMC16FF and GF22FDX chiplets assembled

Wafer-scale integration (hundreds of chiplets)

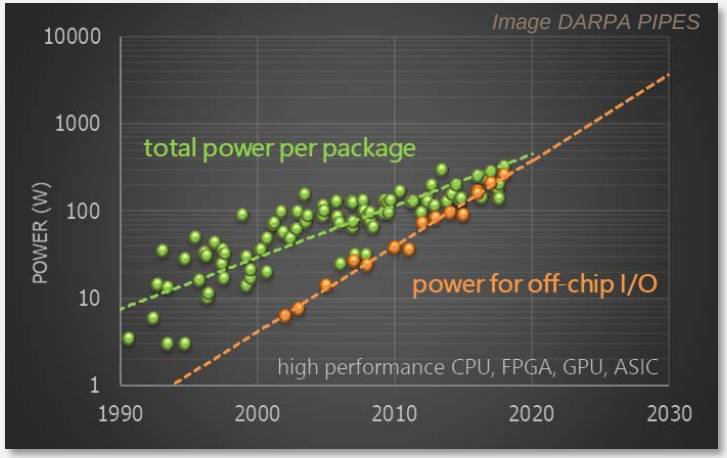


Images: UCLA

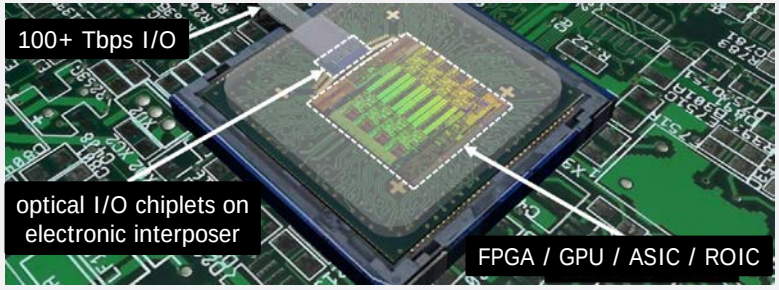
PIPES

PHOTONICS IN THE PACKAGE FOR EXTREME SCALABILITY

Performance Limited by Data Movement

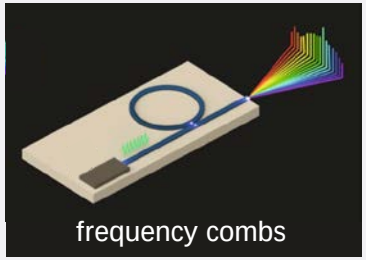


Deployable MCMs with Photonic I/O

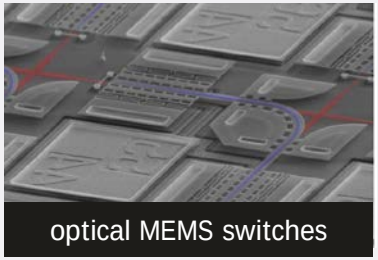


Ayar Labs

Next-Generation Technologies



*Gaeta, Lipson, Kippenberg, Nature Photonics **13**, 158 (2019).*



UC Berkeley

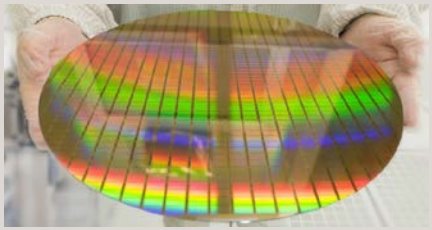
GOALS

- ✓ **Increase socket I/O bandwidth, efficiency, and reach by 100x**
- ✓ **Enable disruptive system parallelism and performance scaling**

LUMOS

LASERS FOR UNIVERSAL MICROSCALE OPTICAL SYSTEMS

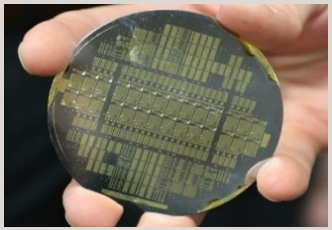
Best Photonic Circuits (Si, $LiNbO_3$, SiN)



X Gain
- no native gain due to material limitations

✓ Photonics
- excellent yield and manufacturability

Best Lasers (GaAs, InP, GaN)



✓ Gain
- discrete lasers & amplifiers
- high power, efficiency & lifetime

X Photonics
- low density & low yield
- high optical losses

LUMOS

intimate integration of gain materials and high-performance photonics

Scaling Complexity with Gain

Gain: Many efficient, high-density gain blocks

Photonics: Advanced process with foundry access

High Power Gain

Gain: Watt-class lasers and amplifiers

Photonics: Fast analog components with low loss

Broad Spectrum Gain

Gain: Narrow linewidth across a wide spectrum

Photonics: Full functionality over visible wavelengths

Images from shutterstock, innovationorigins.com

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Q&A - Discussion

Sarah Leeper

Sarah Leeper is the Director of Secure & Assured Systems at Draper, where she is responsible for Draper's DoD Cyber, Anti-Tamper, and Trusted Microelectronics portfolio. Over the last 18 years, Sarah has held a variety of technology and business strategy positions at innovation forward companies like MIT Lincoln Laboratory, Mercury Systems and CSPi. In these roles, she has had the unique opportunity to bring state of the art commercial and defense specialized technologies to meet the needs of our nation's most challenging microelectronics problems. The technological and economic complexities of these problems continue to be the drive behind her interests. She holds degrees in both Computer Engineering and Neuroscience from the University of Pittsburgh, and a MBA from Southern New Hampshire University.

DRAPER®

Heterogeneous Integration Framework

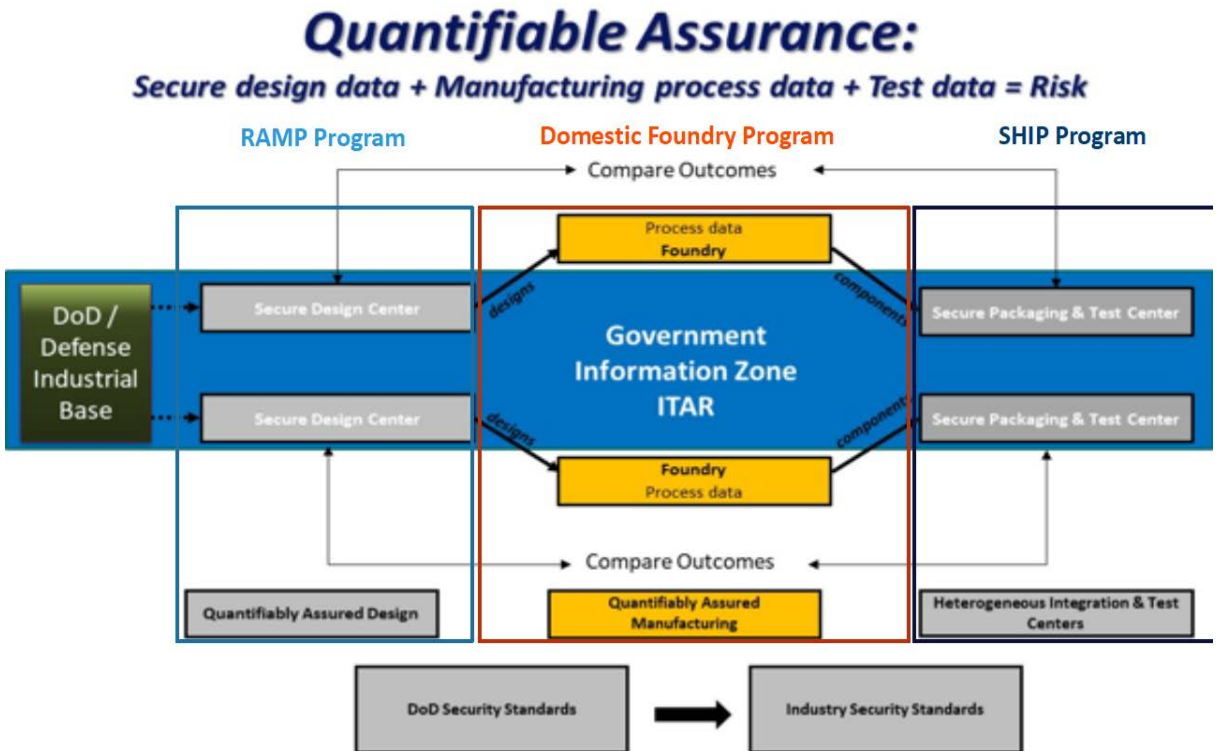
Specialization & Customization of Commercial Components for USG

Sarah Leeper, Director, Secure & Assured Systems

The Charles Stark Draper Laboratory, Inc.
555 Technology Square, Cambridge Mass. 02139-3563 CAGE Code: 51993

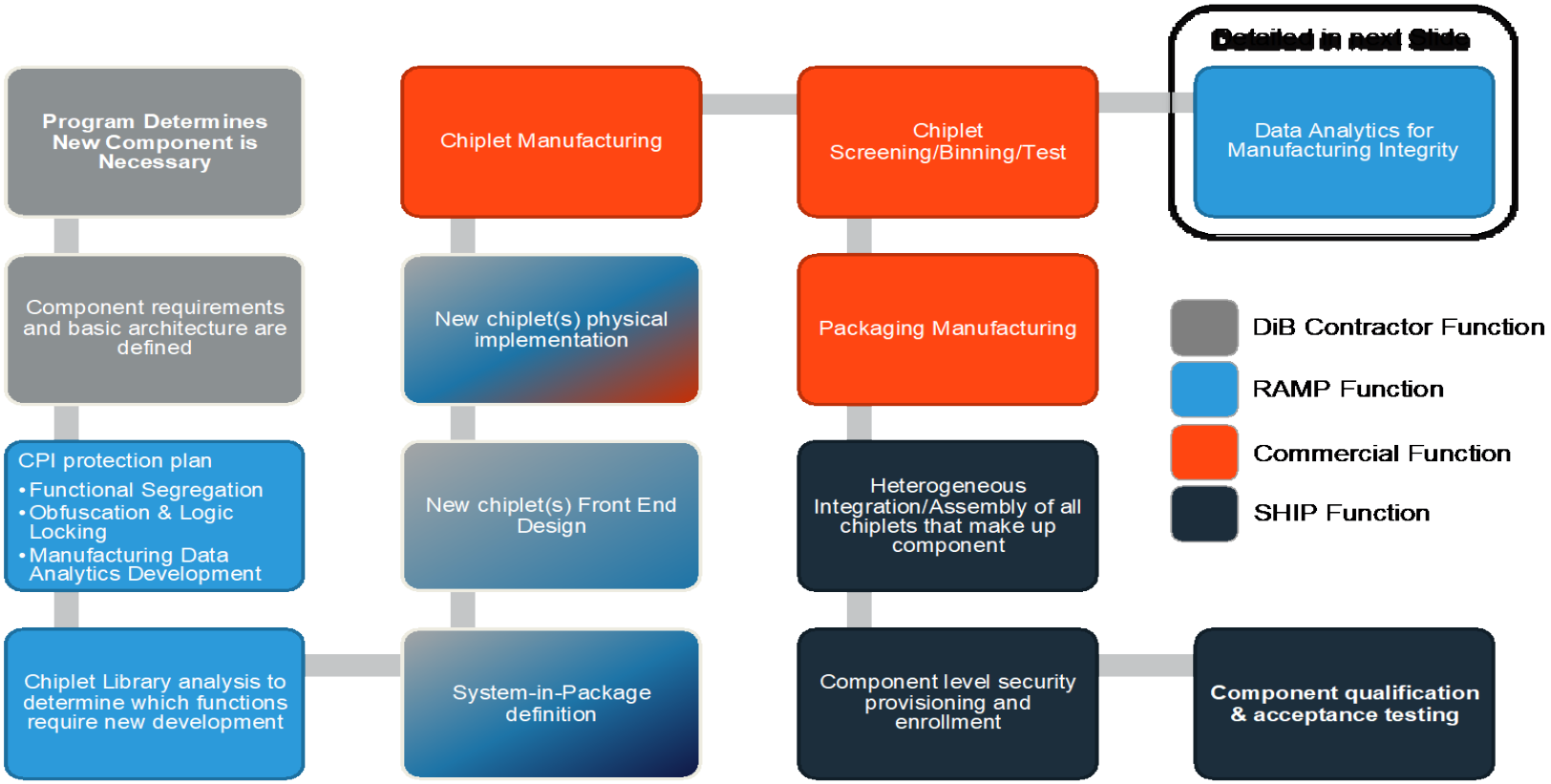
OSD Ecosystem for SOTA Devices

Secure Design and Heterogeneous Integration

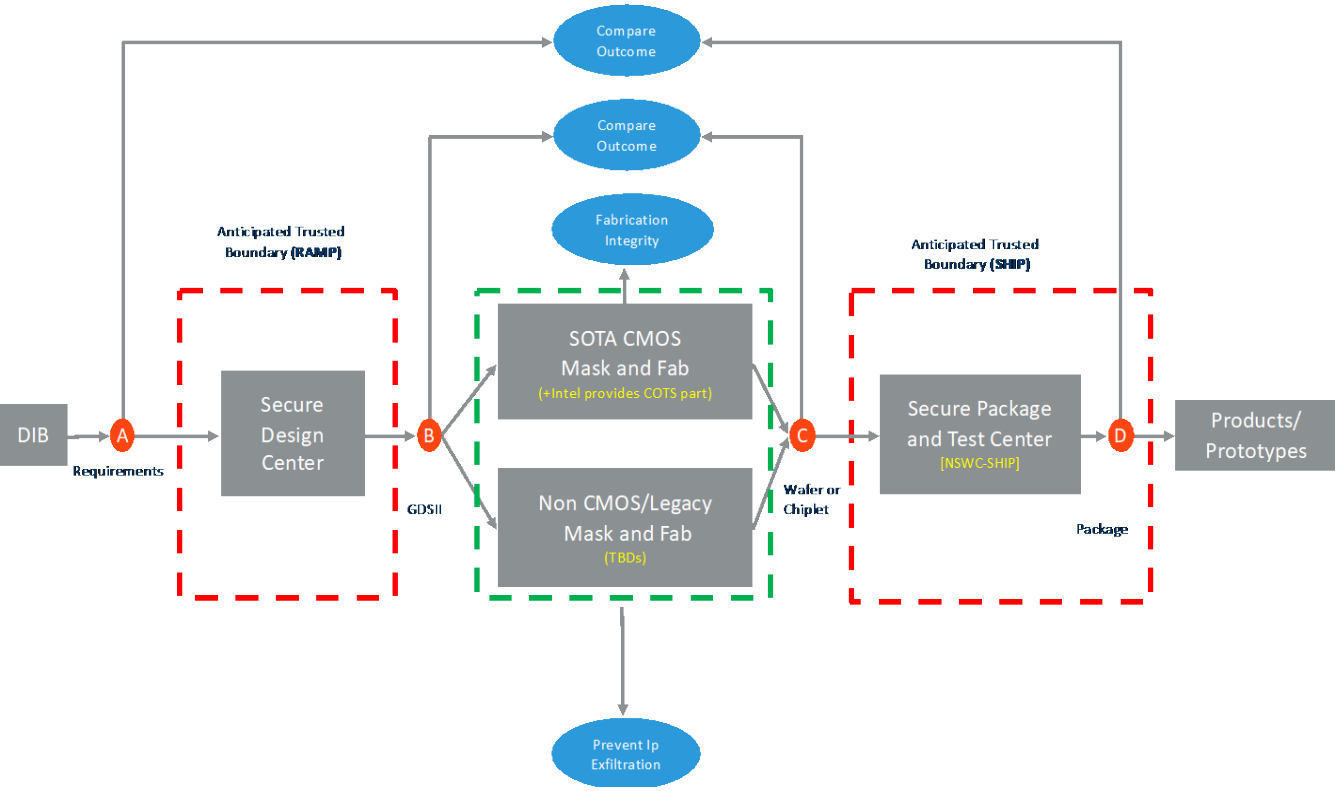


- Optimizing SOTA secure design center flow to SOTA secure packaging
  - Enable design & assembly for USG and DIB contractors
  - Maintain necessary capabilities in a Trusted domestic facility
- Supporting commercial partners to develop transition USG designs to fabrication using SOTA technology, removing ITAR concerns by August 2021

Ecosystem Process Flow



Minimizing risk for manufacturing test



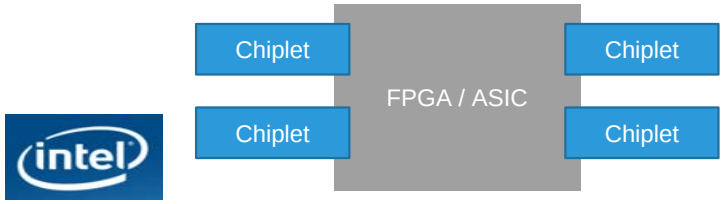
To access the commercial fabs, extra verification & assurance is added at 4 locations.

- Trusted zones around design and packaging
- Novel assurance processes to secure IP and material as it transits through a ”zero-trust” environment
- Addressing confidentiality and integrity throughout
- Advanced methods like fabrication integrity inspection or disaggregation for confidentiality when needed

Specialization and Customization for USG

Robust Chiplet Ecosystem for USG Applications

Precision Instrumentation	Mixed Signal for small change detection **(HI3)**
Sensor Suite	IP Protection
RISC-V Complex	Specialized management guidance and control systems
Inherently Secure Processor (ISP)	Cyber secure processing (**SSITH**)

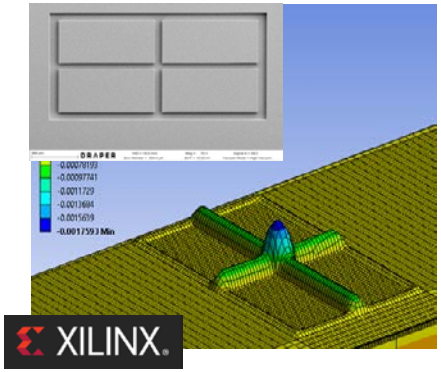


- Disaggregation for flexibility and affordability
- Enabling low volume customization and specialization where necessary through reuse of building block

Innovative Technologies for Commercial Use

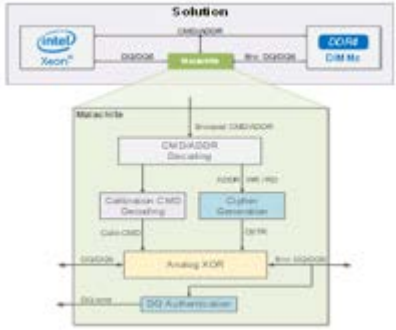
Fragility Structures

Supply Chain Security Solutions (**SHIELD**)



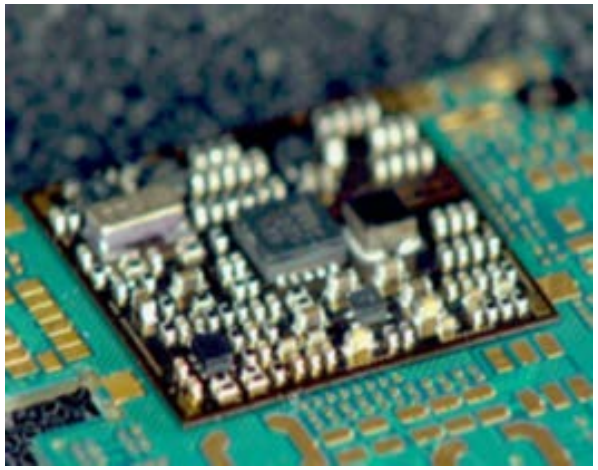
Zero-Latency In-line Encryption ASIC

Full DDR Memory encryption without impact to x86 performance (in development)



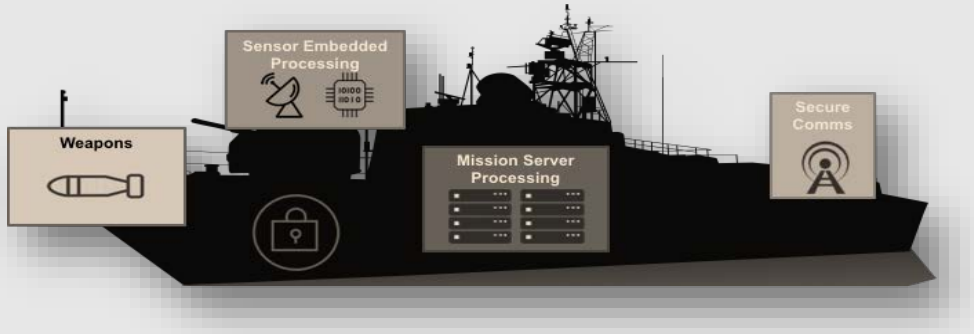
- Infusion of technologies that have commercial value
- Enhance & bridge disruptive R&D into domestic production

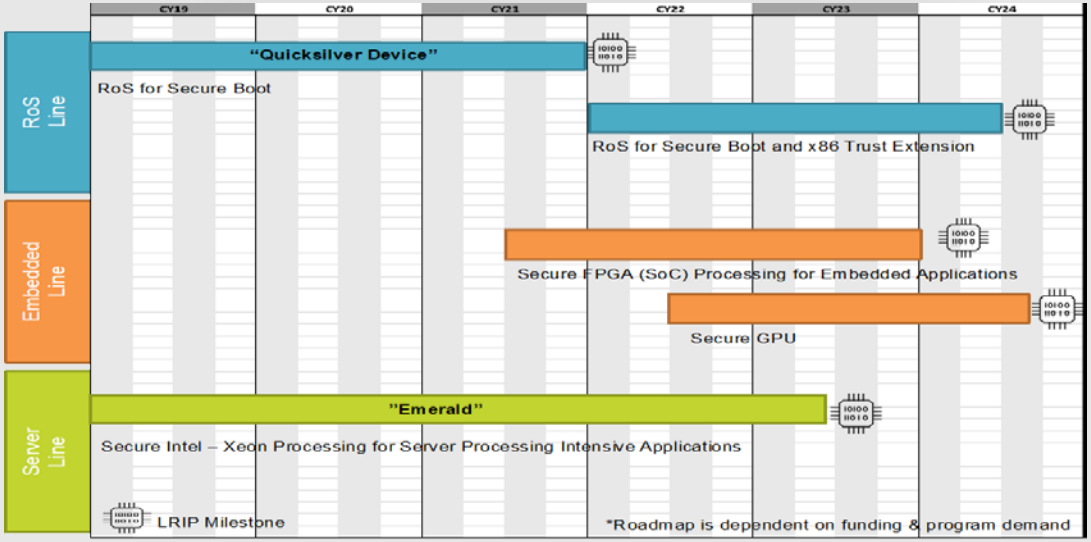
USG Heterogeneous Secure Processing Solutions



i3 microsystems

Packaging Partner for Integrated Ultra High Density (iUHD)





OUSD R&E & Navy Funded efforts for family of qualified parts

Summary

1. Enable development of **Security System Architectures** & Roadmaps to meet mission, cost, & schedule objectives

2. Develop **Government Owned Advanced Packaging** Security Solution Sets for rapid adoption and transition within the market

3. Collaborate on ecosystem development with ***both*** DIB and commercial partners to **adopt** and **transition** solutions and enhance US **microelectronic resiliency**

Chiplet development and reuse of proven and tested IP Blocks for multiple DIB POR

Family of secure processing components Composed through advanced packaging techniques.

Drive Innovation for both commercial and DIB areas of interest

Access to Advanced Packaging and Test
Workshop Agenda

Introduction

Brett Hamilton, Naval Surface Warfare Center (NSWC) Crane, Advanced Packaging and Test, Technical Execution Lead

Panel Members:

- Meredith Anderson Dyck, PhD, Acting Technical Director, NSA Laboratory for Physical Sciences
- Frank Ferrante, Director Military, Aerospace and Government, Intel PSG
- Radoslav (Rocco) Bogoslovov, PhD, Principle Scientist, SETA, DARPA MTO
- Sarah Leeper, Director, Secure & Assured Systems, Draper
- Steven Dooley, Senior Engineer, AFRL Sensors Directorate

Q&A - Discussion

Steven Dooley

Steven Dooley is a Senior Engineer at the Air Force Research Laboratory Sensors Directorate, Aerospace Components and Subsystems Division, Trusted Electronics Branch. Mr. Dooley has a bachelors in mechanical engineering from Wright State University in 2002, and an MBA from Wright State University in 2010. He has been with AFRL since 2002 where he served as the Advanced Packaging lead for the Highly Integrated Microsystems Branch until 2017 where he stood up packaging capabilities for design, pcb fabrication, and advanced assembly for RF and digital applications. He is currently serving as the Advanced Packaging lead for the Trusted Electronics Branch developing a Packaging strategy for fine pitch solutions.

AFRL Advanced Packaging

Name - Steven Dooley
Trusted Electronics Branch, Sensors Directorate AFRL/RYDT

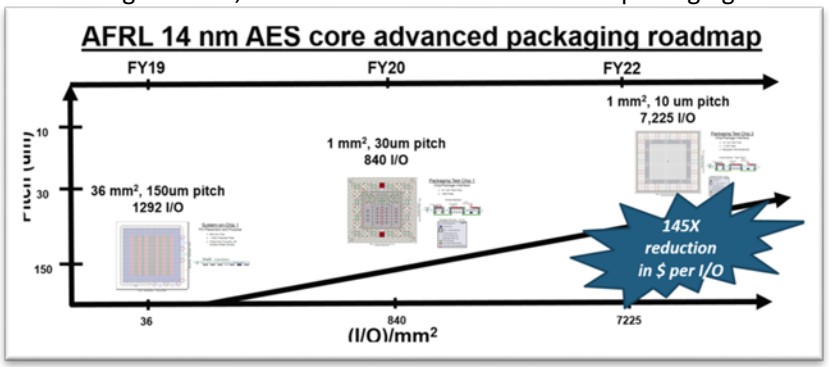
Position - Senior Engineer

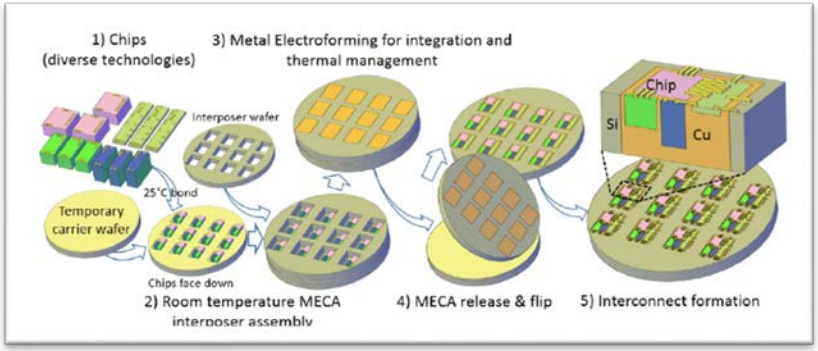
Event – ERI
Date – 8/20/2020

Strategy to Task: Advanced Packaging for Innovation

Enable access to secure, domestic Heterogeneous Integration/ Fan Out Wafer Level Packaging (FOWLP) technologies. Key goal to drive down the I/O cost per mm2 for advanced technology nodes

- Leverage AFRL internal efforts and facilities in advanced packaging from Heterogeneous Integration (HI) and ROIC Teams
  - Explore 2 fine-pitch technology solutions: 1) HI/FOWLP technology 2) Fine pitch bumping on singulated die with interposer
- Leverage DARPA, Title III investments in advanced packaging





Metal Embedded Chip Assembly (MECA) enables high density multi-chip 2.5/3D HI integration for RF and fine pitch digital applications

Three main activities for HRL transfer/ process innovation

1. **MECA Tech transfer** - Current MECA process from HRL to AFRL/RY cleanroom facility
2. **Digital MECA** - Process innovation that will allow for multi-layer fine pitch fan out (FOWLP) for digital IC's with 1000's of I/O
3. **T (temporary) MECA** - Fine pitch bumping on singulated IC's down to 1mm^2 with 10 um pitch utilizing a fine pitch interposer substrate.

Access to Advanced Packaging and Test
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Advanced Packaging and Test

Q&A -

Discussion